Abstract of the Disclosure:

A wafer test apparatus for bringing the contact areas of the integrated circuits to be tested into electrical connection with the test contacts as uniformly as possible and therefore with relatively low necessary contact pressures. The test apparatus has a chuck for holding a wafer having at least one integrated circuit with a group of contact areas which define a wafer surface profile. A test head is configured opposite the chuck and has a performance board, on which a probe card with contacts for making contact with the contact areas of the integrated circuit is configured. Areas of the contacts, of the probe card, which are intended to come into contact with the contact areas define a test surface profile. Actuators are configured on the probe card for aligning the test surface profile in parallel with the wafer surface profile and for changing the distance between the performance board and the contacts in a direction substantially orthogonal to the wafer surface profile.

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